Build & maintain FPGA applications for finance

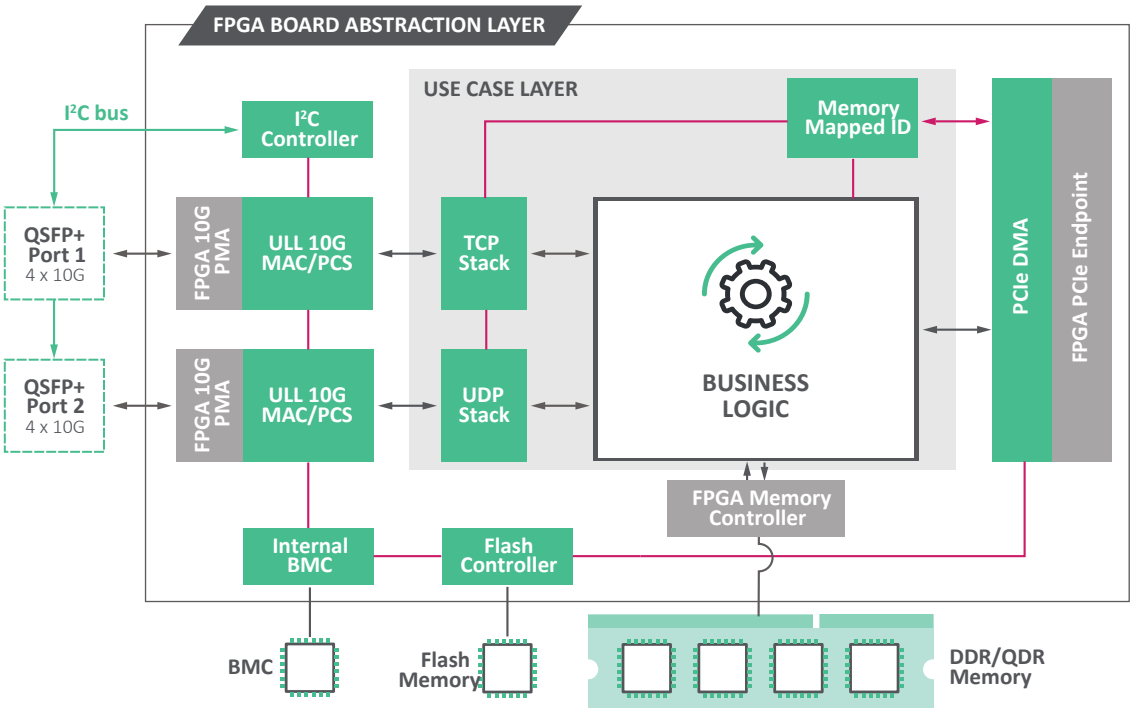
nxFramework

What is nxFramework?

The Enyx Development Framework (nxFramework) is a hardware and software development environment designed to efficiently build and maintain ultra-low latency FPGA network applications for the financial industry.

Based on 10 years of research and development, nxFramework is the foundation for all Enyx off-the-shelf solutions and provides our clients with the toolchain to manage a large portfolio of applications.

Developed for building in-house high performance trading engines, order execution systems, pre-trade risk check gateways, and custom projects — the nxFramework offers:



What types of IP cores are included?

Ultra-low latency connectivity cores

- 10G MAC/PCS **29ns RTT - SOP to SOF @ 322MHz**
- 40G MAC/PCS **55ns RTT - SOP to SOF @ 322MHz**
- 10G TCP stack **53ns RTT @ 322MHz**
- 10G UDP stack **43ns RTT @ 322MHz**
- PCIe streaming DMA **790ns RTT @ 250MHz**

Library of 60+ utility cores

- MMIO core library
- Packet streaming core library
- Memory managment core library
- Math core library
- Statistics core library
- Simulation helpers library

Check out all our performance reports for full testing details
www.enyx.com/performance

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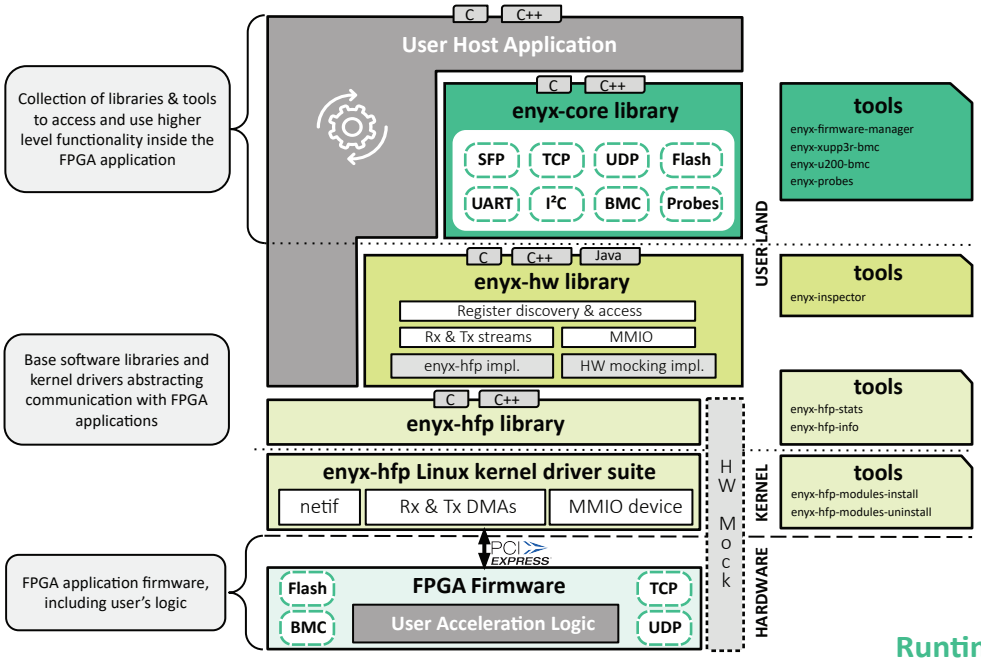
Key Features:

Runtime Software Stack
Enables simple configuration and monitoring of Enyx connectivity & utility cores, including interaction with the FPGA application via our C/C++ libraries.

Hardware Development Environment
A Python scripted development environment that enables users to simplify their development cycle and accelerate their time-to-production.

Platform Mobility: Flexible & Future-Proof
Supported across the multiple platforms, nxFramework is not restrained by current or future technology updates.

The Enyx Inspector: Efficient Debugging
Equipped with a web-based GUI that can configure and monitor the FPGA at runtime, allowing for quick deployment and debug.



Runtime Software Stack

Specifications:

The following connectivity cores are provided:
- 10G/40G Ultra Low Latency MAC/PCS
- 1G/10G Full TCP stack
- 1G/10G Full UDP stack
- ULL PCIe Streaming DMA

Board management cores:
- Flash controller support for FPGA bitstreams
- I²C bus controller for SFP/QSFP communication
- Configurable instantiation of memory controllers (DDR4, QDR II+)

Additional elements included:
- The Enyx Inspector: a web-based debugging tool
- Linux drivers & configuration/communication libraries
- Off-the-shelf, configurable reference designs
- Support for widely used FPGA families in the financial

Certified Hardware Platform Partners

ARISTA

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Evolve Past Latency.

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