

# Build & maintain FPGA applications for finance

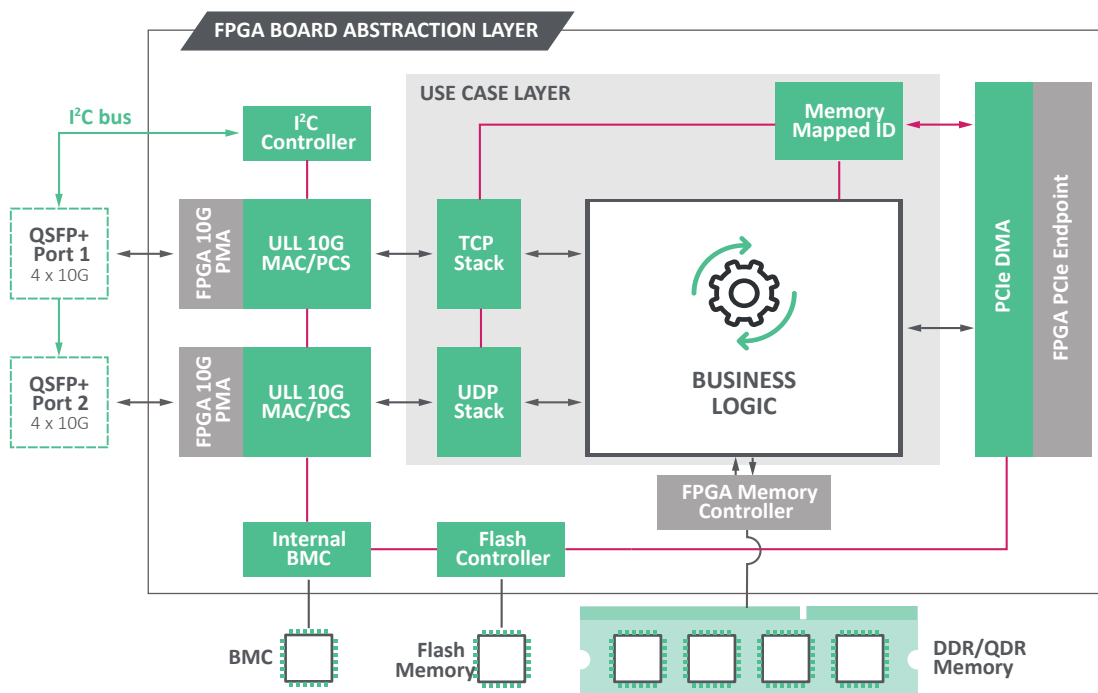
## nxFramework

### What is nxFramework?

The Enyx Development Framework (nxFramework) is a hardware and software development environment designed to efficiently build and maintain ultra-low latency FPGA network applications for the financial industry.

Based on 10 years of research and development, nxFramework is the foundation for all Enyx off-the-shelf solutions and provides our clients with the toolchain to manage a large portfolio of applications.

Developed for building in-house high performance trading engines, order execution systems, pre-trade risk check gateways, and custom projects — the nxFramework offers:



### What types of IP cores are included?

#### ULTRA-LOW LATENCY CONNECTIVITY CORES

- 10G MAC/PCS **29ns RTT - SOP to SOF @ 322MHz**
- 40G MAC/PCS **55ns RTT - SOP to SOF @ 322MHz**
- 10G TCP stack **53ns RTT @ 322MHz**
- 10G UDP stack **43ns RTT @ 322MHz**
- PCIe streaming DMA **790ns RTT @ 250MHz**

#### LIBRARY OF 60+ UTILITY CORES

- MMIO core library
- PCIe streaming DMA
- Packet streaming core library
- Memory management core library
- Math core library
- Statistics core library
- Simulation helpers library

# Key Features

## » Runtime Software Stack

Enables simple configuration and monitoring of Enyx connectivity & utility cores, including interaction with the FPGA application via our C/C++ libraries.

## » Platform Mobility: Flexible & Future-Proof

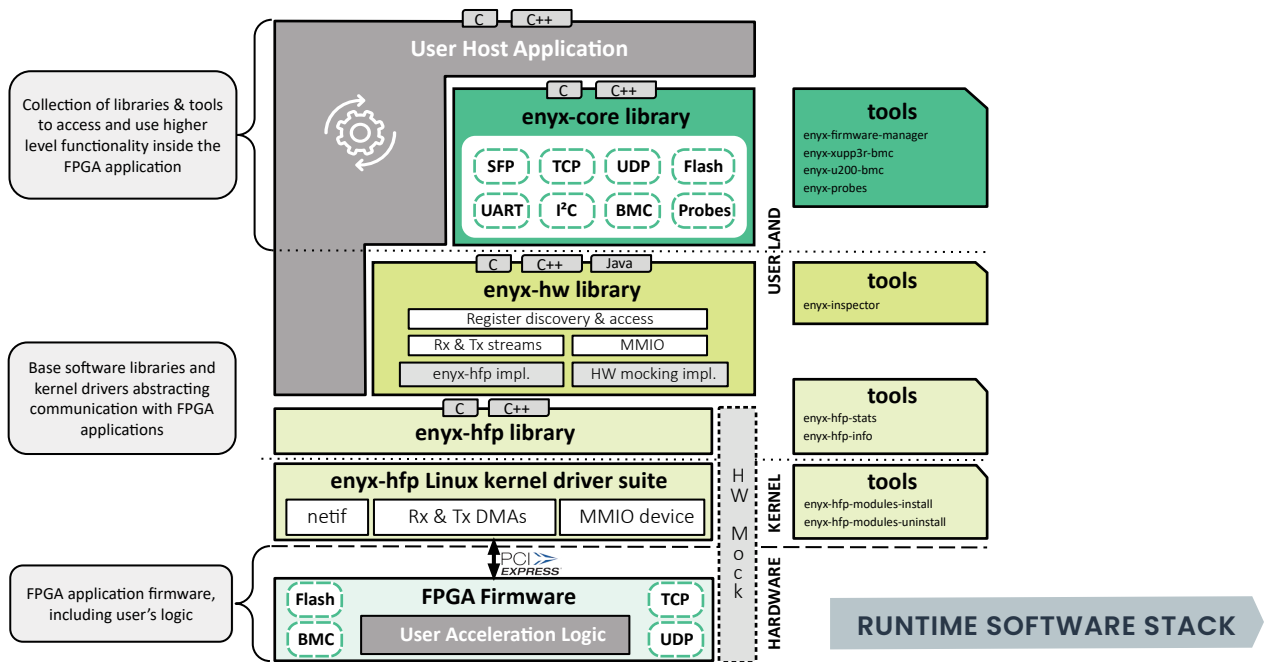
Supported across the multiple platforms, nxFramework is not restrained by current or future technology updates.

## » Hardware Development Environment

A Python scripted development environment that enables users to simplify their development cycle and accelerate their time-to-production.

## » The Enyx Inspector: Efficient Debugging

Equipped with a web-based GUI that can configure and monitor the FPGA at runtime, allowing for quick deployment and debug.



# Specifications

## The following connectivity cores are provided:

- 10G/40G Ultra Low Latency MAC/PCS
- 1G/10G Full TCP stack
- 1G/10G Full UDP stack
- ULL PCIe Streaming DMA

## Board management cores:

- Flash controller support for FPGA bitstreams

- I2C bus controller for SFP/QSFP communication
- Configurable instantiation of memory controllers (DDR4, QDR II+)

## Additional elements included:

- The Enyx Inspector: a web-based debugging tool
- Linux drivers & configuration/communication libraries

- Off-the-shelf, configurable reference designs
- Support for widely used FPGA families in the financial

## Certified Hardware Platform Partners

ARISTA

**BittWare**  
a molex company

**AMD**

Evolve Past Latency. [www.enyx.com/nxFramework](http://www.enyx.com/nxFramework)

